REMARKS

Applicants respectfully request that the Claims in the above-identified patent application be reconsidered and again examined in view of the following remarks.

Applicant respectfully requests that the correction to the drawings as submitted to the Chief Draftsman be approved. Applicant has corrected Figures 1 and 2 as suggested by the Examiner by designating the figures as Prior Art as shown in red on the enclosed copies.

Applicant has provided a new title that is indicative of the invention to which the claims are directed.

Claim 5 has been amended to correct the antecedent basis problem for the limitation "such package."

Claims 1-7 were pending in the application. Claims Applicant has amended Claims 1, 3, and 5-7. Applicant has cancelled Claim 2 and 4 and added new claims 10-15. No new matter has been added.

The Examiner rejected Claims 1, 5-6 and 7 under 35 U.S.C. 102(b) as being as being anticipated by Murari et al. (US 5,696,404). The Examiner rejected Claims 1-4 and 6 under 35 U.S.C. 102(b) as being as being anticipated by Tagaya (JP 6-13447). The Examiner rejected Claims 1-4 and 6-7 under 35 U.S.C. 102(e) as being as being anticipated by Egawa (US 6,066,886).

Amended Claim 1 recites: " a plurality of voltage generators." Applicant respectfully submits that Murari neither suggests nor discloses a plurality of voltage generators. Referring to Tagaya, the Office Actions states "wherein each one of the electrical components 10 is voltage

signal generators (see abstract)." Applicants' amended Claim 1 recites a plurality of voltage generators while the abstract of Tagaya refers to block 10 as an auxiliary circuit 10 which processes a test signal to be measured. Applicant respectfully submits that the auxiliary circuit of Tagaya would not be considered as a voltage generator by one of ordinary skill in the art. Likewise the redundant memory portion 4 of Egawa is not a voltage generator. Independent Claim 1 is neither described nor suggested by the references since the references taken separately or in combination neither describe nor suggest a plurality of voltage generators.

Dependent Claim 3 adds the limitation "each one of the voltage generators is disposed in the separating region" to claim a further patentably distinct feature of the invention.

Dependent Claim 5 adds a further patentably distinct feature of the invention reciting "such electrical conductor being elevated above the regions in the fractional portion of the wafer."

Amended Claim 6 recites "an electrical conductor electrically connecting the plurality of electrical selected one or ones of the electrical components to the chips with portions of the electrical conductor elevated above the regions in the fractional portion of the wafer." Murari, Tagaya and Egawa disclose electrical conductors which are integral to the wafer. Applicants' electrical conductor is provided separate from the wafer and is thus elevated above the regions in the fractional portion of the wafer. Independent Claim 6 is neither described nor suggested by the references since the references taken separately or in combination neither describe nor suggest an electrical conductor which is elevated above the regions in the fractional portion of the wafer.

Dependent Claim 7 adds a further patentably distinct feature of the invention reciting "wherein each set of electrical components includes a plurality of different electrical components."

Applicants' new Claim 10 recites "a fusible link electrically connecting a bus disposed in at least one of the plurality of integrated circuit chips and a corresponding one of the plurality of electrical components." Applicants respectfully submit that none of the cited references suggest or disclose such an arrangement. Applicants have added new Claims 11 through 15. These Claims recite further patentable distinct aspects of the invention.

Applicant submits that all of the claims are now in condition for allowance, which action is requested.

Authorization to charge Daly, Crowley & Mofford, LLP Deposit Account No. 50-0845 for any excess fees due or credit any overpayment is hereby given.

Respectfully submitted,

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Attachment: 2 Sheets of Claims with markings showing changes made, copy of letter to Chief Draftsman.

Version of Specification and Claims with Markings to Show Changes Made

The Title

MULTIPLE CHIP SEMICONDUCTOR ARRANGEMENT HAVING ELECTRICAL COMPONENTS IN SEPARATING REGIONS

In the Claims

1. (Amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of ~~electrical components~~voltage generators, each one being associated with, and adjacent to, a corresponding one of the chips.

~~2. The semiconductor recited in claim 1 wherein the electrical components are voltage generators.~~

3. (Amended) The semiconductor recited in claim 2 wherein each one of the ~~components~~ voltage generators is disposed in the separating region~~,~~.

~~4. The semiconductor recited in claim 3 wherein the electrical components are voltage generators~~

5. (Amended) The semiconductor recited in claim 1 wherein each one of the voltage generators has an electrical contact and wherein ~~such package~~the semiconductor further includes:

a dielectric member having an electrical conductor thereon, such electrical conductor being elevated above the regions in the fractional portion of the wafer and electrically connected to the plurality of electrical contacts of the plurality of chips to electrically

interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer.

6. (Amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

an electrical conductor electrically connecting the plurality of electrical selected one or ones of the electrical components to the chips with portions of the electrical conductor elevated above the regions in the fractional portion of the wafer and spanning the separating regions between the chips in the fractional portion of the wafer.

7. (Amended) The semiconductor recited in claim 6 wherein each set of electrical components includes ~~having~~ a plurality of different electrical components.